(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 963 073 A1

(12) EUROPEAN PATENT APPLICATION

published in accordance with Art. 158(3) EPC

(43) Date of publication:
08.12.1999 Bulletin 1999/49

(21) Application number: **98961361.7**

(22) Date of filing: **16.12.1998**

(51) Int. Cl.[6]: **H04L 1/00**, H04J 3/00

(86) International application number:
PCT/JP98/05680

(87) International publication number:
WO 99/31836 (24.06.1999 Gazette 1999/25)

(84) Designated Contracting States:
DE FR GB NL

(30) Priority: **16.12.1997 JP 36403797**

(71) Applicant: **NIPPON HOSO KYOKAI**
Tokyo 150-8001 (JP)

(72) Inventors:
- **Hashimoto, Akinori**
  Setagaya-ku, Tokyo 157-8510 (JP)
- **Katoh, Hisakazu,**
  NHK Broadcasting Ctr.
  Tokyo 150-8001 (JP)
- **Matsumura, Hajime**
  Setagaya-ku, Tokyo 157-8510 (JP)
- **Kumada, Junji**
  Setagaya-ku, Tokyo 157-8510 (JP)

(74) Representative:
Beresford, Keith Denis Lewis
2-5 Warwick Court
High Holborn
London WC1R 5DJ (GB)

(54) TRANSMITTER AND RECEIVER

(57) An interleave frame is formed by combining slots corresponding to the same slot number in each frame when interleave process is performed in a super frame, and the data are read out along row or column direction (i.e. readout direction) and the data are written along the direction opposite to the readout direction in the same memory.

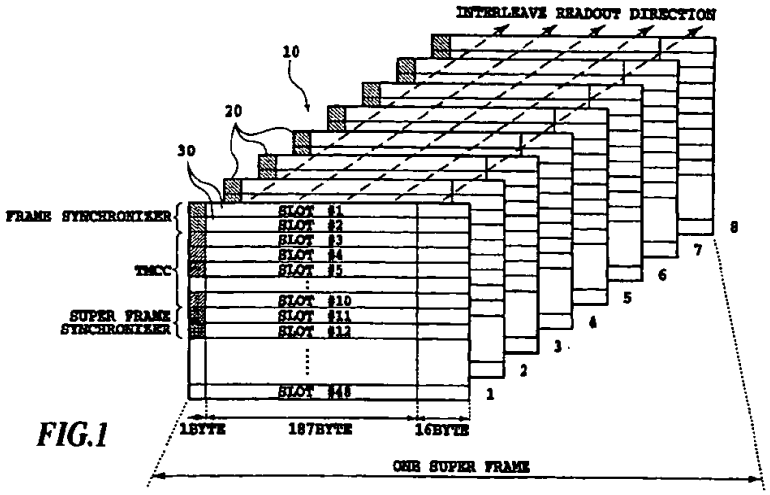

FIG.1

EP 0 963 073 A1

Description

TECHNICAL FIELD

[0001] The present invention relates to an interleaving technique involved in digital modulation and demodulation, especially to a transmitter and a receiver capable of performing the unified interleave and deinterleave without employing interleave method corresponding to multiplexing scheme based on each transmission mode when implementing multiplex transmission combining a plurality of transmission modes with different error endurance.

BACKGROUND ART

[0002] Fig. 4 shows a multiplexed signal structure in which a frame structure is comprised of one frame including 48 slots and one super frame is structured by eight frames, for example. Here, a slot is a memory area for storing a packet consisting of 204 bytes adding a 16-byte RS(204,188) error correction code to a 188-byte MPEG-2 TS packet. In digital transmission using a broadcasting satellite, it is assumed that the slots of the same number of each frame in a super frame may use the same type transmission mode including modulation scheme and error correction code, and four types of transmission modes can be used at maximum in one super frame. In addition, the transmission modes in the super frame are flexibly varied by reporting those modes from a transmitting side to a receiving side by using a control signal called TMCC signal contained in second previous super frame.

[0003] Fig. 5 shows the structure of a modulated signal generated from the multiplexed signal. In this case, the multiplexed data is subjected to interleaving in the transmitter side and deinterleaving in the receiving side in order to derive the full power of Reed-Solomon (RS) codes, typical external codes, by distributing burst errors which is occurred when the number of bit errors in transmission channel is beyond the error correcting capability of a Viterbi decoder or a trellis decoder used for error correction in the receiver. For example, interleaving of depth eight is implemented by forming interleave frames as every eight slots using the same type transmission mode in a frame, and by reading out of column the data of the interleave frames written into row in a two-dimensional memory. (When the number of the slots using the same type transmission mode is less than eight in the frame, or the number of the remaining slots is less than eight when the interleave frames are formed every eight slots in sequence, the interleave frame is structured in addition to slots of a frame which will be described later.)

[0004] As structural examples, implementing interleave process will now be described with reference to Figs. 6 and 7. Fig. 6 shows an example in which 46 slots are transmitted by TC-8 PSK and one slot is transmitted by QPSK subjected to convolutional encoding with a coding rate 1/2, and further, one slot is regarded as a dummy slot. Fig. 7 shows an example in which 44 slots are transmitted by TC-8 PSK and one slot is transmitted by BPSK subjected to convolutional encoding with a coding rate 1/2, and further, three slots are regarded as dummy slots.

[0005] In either example, as for the one slot transmitted by QPSK or BPSK, one interleave frame is formed in one super frame. To match the timing of signals after the interleaving, a first-in-first-out (FIFO) memory for storing data with a length of super frame {(data length of assigned slots) - (length of the interleave frame)} is necessary for the greater assigned slot number (in the above example, the 46 slots or 44 slots data transmitted by the TC-8 PSK).

[0006] Since the interleave frame is 204×8 bytes, a FIFO memory is comprised of 204×46×8-204×8=73440 bytes in the example of Fig. 6, and shows a FIFO memory is comprised of 204×44×8-204×8=70176 bytes in the example of Fig. 7, thus performing the interleave process by once storing the data amount close to one super frame every each transmission mode.

[0007] However, the capacity of the FIFO memory changes according to the assigned slot number for each of transmission modes in the frame, and a controller controlling the interleave process should be needed because address control is changed according to the change of the capacity of the FIFO memory, thereby complicating a circuit structure.

DISCLOSURE OF THE INVENTION

[0008] Therefore, an object of the present invention is to provide a transmitter and a receiver implementing a interleave process simply without changing the circuit configuration by changing the assigned slot number according to the transmission mode in each frame.

[0009] In the first aspect of the present invention, there is provided a transmitter applicable to a transmission system capable of transmitting digital data (called transmission coded signal), which are encoded by using some different types of error correction code and are modulated by some different types of modulation schemes, as packet unit in the multiplexed data with a frame structure consisting of N packets, said transmitter performing interleave as super frame unit, said transmitter comprising:

means for forming a interleave frame by combining packets corresponding to the same slot number in each frame;

write means for sequentially writing data according to a frame number of the interleave frame into a two-dimensionally arrangeable memory along row or column direction; and

readout means for sequentially reading out the written data from the two-dimensionally arrangeable memory along a direction (i.e. column or row direction) different from the written direction based on said write means.

[0010] In the second aspect of the present invention, there is provided a transmitter applicable to a transmission system capable of transmitting digital data (called transmission coded signal), which are encoded by using some different types of error correction code and are modulated by some different types of modulation techniques, as packet unit in the multiplexed data with a frame structure consisting of N packets, said transmitter performing deinterleave as super frame unit, said transmitter comprising:

means for forming a deinterleave frame by combining packets corresponding to the same slot number in each frame;

write means for sequentially writing data according to a frame number of the deinterleave frame into a two-dimensionally arrangeable memory along the same direction (i.e. column or row direction) corresponding to the readout direction of interleave process on the transmission occasion; and

readout means for sequentially reading out the written data from the two-dimensionally arrangeable memory along the direction (i.e. row or column direction) which is different from the written direction based on said write means and is corresponding to the written direction of the interleave process on the transmission occasion.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]

Fig. 1 is a schematic perspective view showing a frame structure as an embodiment according to the present invention;

Fig. 2 is a diagram showing data arrangement in frames according to the present invention;

Fig. 3 is a diagram showing an example of an interleave process;

Fig. 4 is a schematic perspective view showing a conventional frame structure;

Fig. 5 is a diagram showing data arrangement in conventional frames;

Fig. 6 is a block diagram showing a conventional transmission process; and

Fig. 7 is a block diagram showing another conventional transmission process.

BEST MODE FOR CARRYING OUT THE INVENTION

[0012] Preferred embodiment of the present invention will be described in detail with reference to the drawings.

[0013] The present invention relates to an interleave process applicable to digital transmission. In particular, in a transmission system that can transmit the mixed data comprising of some different types of transmission modes as packet unit in the multiplexed data with a frame structure consisting of N packets, an interleave frame is formed by combining slots corresponding to the same slot number in each frame, and interleave process is performed every interleave frame, thus simply performing interleave process under the same memory control even though any types of transmission modes in mixed data may be transmitted.

[0014] This example refers to a reading and writing process of a transmission system in that interleave in the transmitter and deinterleave in the receiver, which is opposite to the interleave can be performed. A concrete example will be described as follows.

[0015] Fig. 1 shows the structure of a single super frame 10. The super frame 10 is structured by eight frames 20. Each frame 20 consists of 48 slots 30. These slots 30 are structured by various types of signals, such as multiplexed signals including video, audio and associated informations, a frame synchronizer, TMCC and super frame synchronizer. One slot 30 consists of (1+187+16) bytes. Fig. 2 shows the frames 20 in the super frame 10 sequentially arranged.

[0016] The processings performed by the transmission and reception of the system will be described with reference to Figs. 3(a) to 3(e).

[0017] Fig. 3(b) shows a memory 40 capable of being arrayed in two dimensions. First, when Fig. 3 is assumed to be a process of the transmitter, Fig. 3(a) shows the data arrangement in the super frame 10 before interleave. In contrast, Fig. 3(c) shows the data arrangement after interleave. Figs. 3(d) to 3(e) schematically shows the data read process from the memory 40.

[0018] In the present example, using the memory 40, the interleave process as to the data in the super frame 10 of Fig. 1 is performed. This is to say, the data is written into the memory 40 in the horizontal direction (along row direction), and the data is read out from the memory 40 in the vertical direction (along column direction). More detail example will

be described as follows.

[0019] As an example, when slot number is 1, the interleave is performed as to the slots #1 of the first to eighth frames 20, and the data is written into the two-dimensional memory 40 along row direction sequentially from the first slot of the first frame 20. In the present example, the ith data of each frame 20 (shaded area) is written every 203-byte data width.

[0020] After the data is written, the data is read out from the memory 40 along column direction perpendicular to row direction.

[0021] Table 1 shows actual read address and the data read address of the first slots according to each frame is sequentially arranged. Here, the numerals indicate frame-byte.

[Table-1]

Read addresses of first slots (frame-byte)				
	Start (frame-byte)	Second byte (frame-byte)		203th byte (frame-byte)
first frame	1-1	2-1	...	3-26
second frame	4-26	5-26	...	6-51
third frame	7-51	8-51	...	1-77
fourth frame	2-77	3-77	...	4-102
fifth frame	5-102	6-102	...	7-127
sixth frame	8-127	1-128	...	2-153
seventh frame	3-153	4-153	...	5-178
eighth frame	6-178	7-178	...	8-203

[0022] By doing the readout process, interleave can be performed independently of the assigned slot number every each frame.

[0023] Furthermore, by exchanging the readout direction and the write, deinterleave can be performed in the receiver (i.e. deinterleave process can be performed by writing the data according to the readout direction of interleave and can be performed by reading out the data according to the write direction of interleave).

[0024] On the other hand, when Fig. 3 is assumed to be a process of the receiver, Fig. 3(c) shows the data before the deinterleave process, and Fig. 3(a) shows the data after the deinterleave process.

INDUSTRIAL APPLICABILITY

[0025] As described above, according to the present invention, an interleave frame is formed by combining slots corresponding to the same slot number in each frame when interleave process is performed in a super frame, and the data are read out along row or column direction (i.e. readout direction) and the data are written along the direction opposite to the readout direction in the same memory. This makes it possible to obviate complicated memory address controllers according to transmission mode structures in the interleave or deinterleave process, thereby enabling a uniform control in any cases.

Claims

1. A transmitter applicable to a transmission system capable of transmitting digital data (called transmission coded signal), which are encoded by using some different types of error correction code and are modulated by some different types of modulation schemes, as packet unit in the multiplexed data with a frame structure consisting of N packets, said transmitter performing interleave as super frame unit, said transmitter characterized by comprising:

   means for forming a interleave frame by combining packets corresponding to the same slot number in each frame;
   write means for sequentially writing data according to a frame number of the interleave frame into a two-dimensionally arrangeable memory along row or column direction; and
   readout means for sequentially reading out the written data from the two-dimensionally arrangeable memory along a direction (i.e. column or row direction) different from the written direction based on said write means.

2. A transmitter applicable to a transmission system capable of transmitting digital data (called transmission coded signal), which are encoded by using some different types of error correction code and are modulated by some different types of modulation techniques, as packet unit in the multiplexed data with a frame structure consisting of N packets, said transmitter performing deinterleave as super frame unit, said transmitter characterized by comprising:

means for forming a deinterleave frame by combining packets corresponding to the same slot number in each frame;
write means for sequentially writing data according to a frame number of the deinterleave frame into a two-dimensionally arrangeable memory along the same direction (i.e. column or row direction) corresponding to the readout direction of interleave process on the transmission occasion; and
readout means for sequentially reading out the written data from the two-dimensionally arrangeable memory along the direction (i.e. row or column direction) which is different from the written direction based on said write means and is corresponding to the written direction of the interleave process on the transmission occasion.

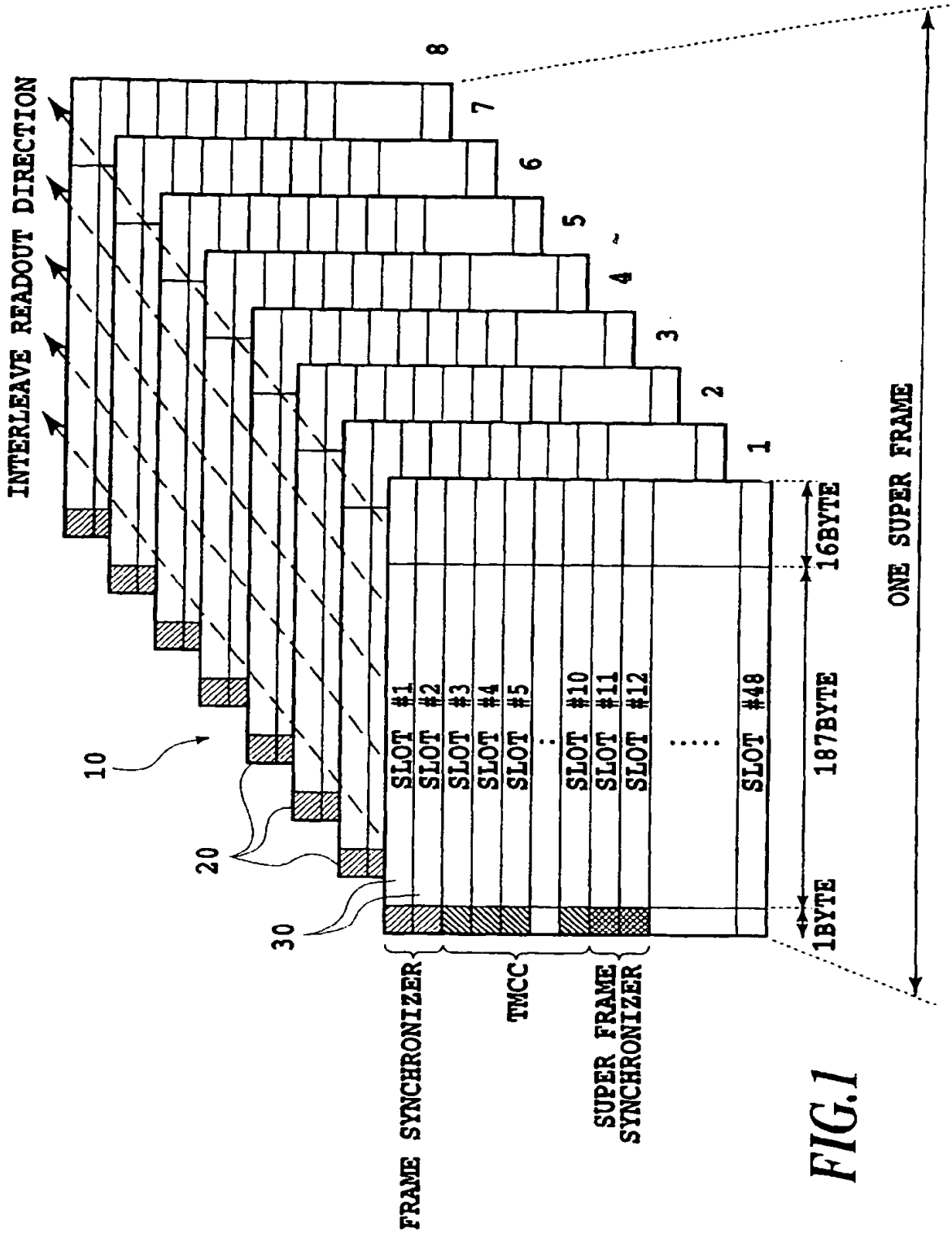

FIG.1

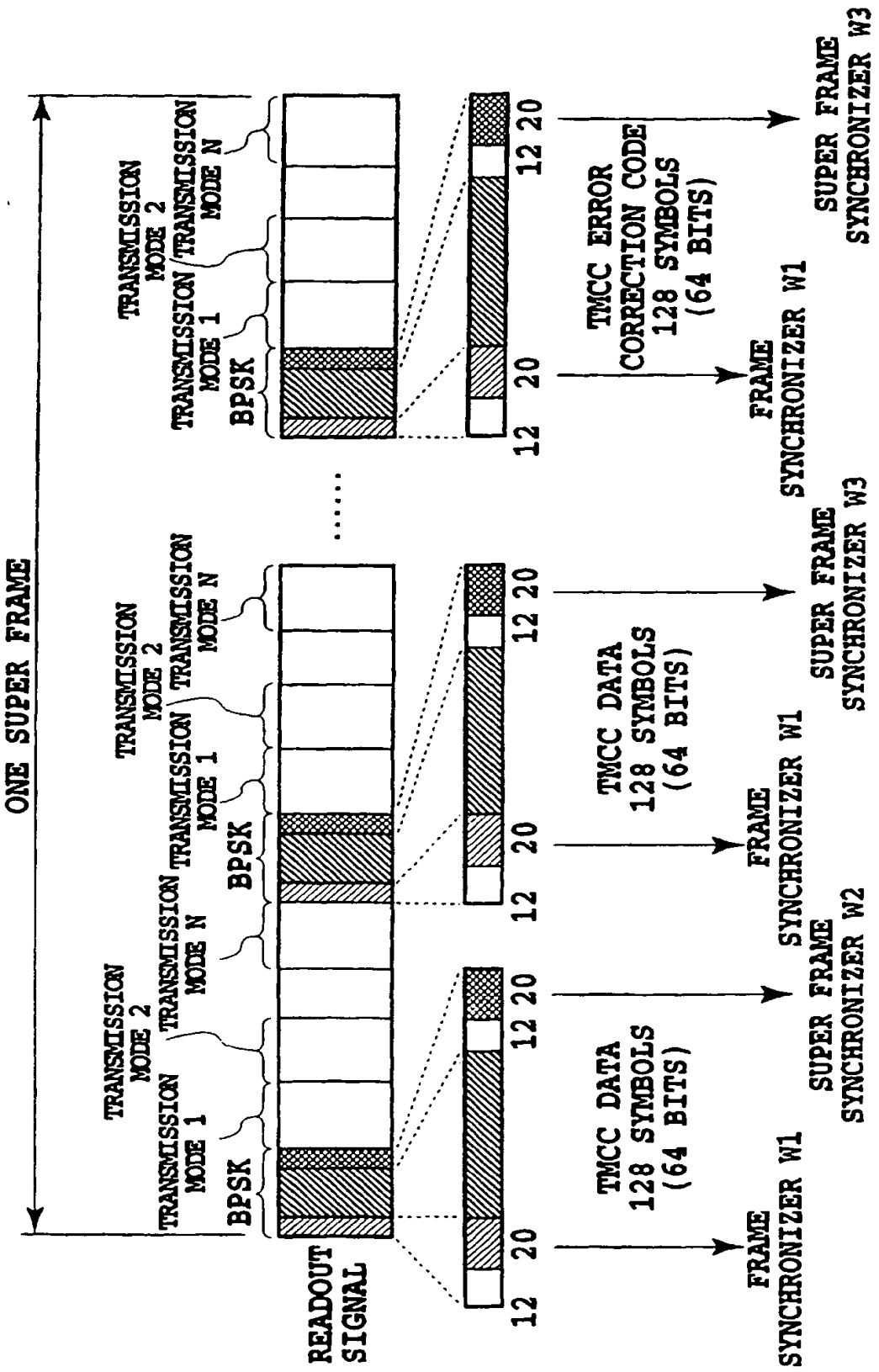

FIG.2

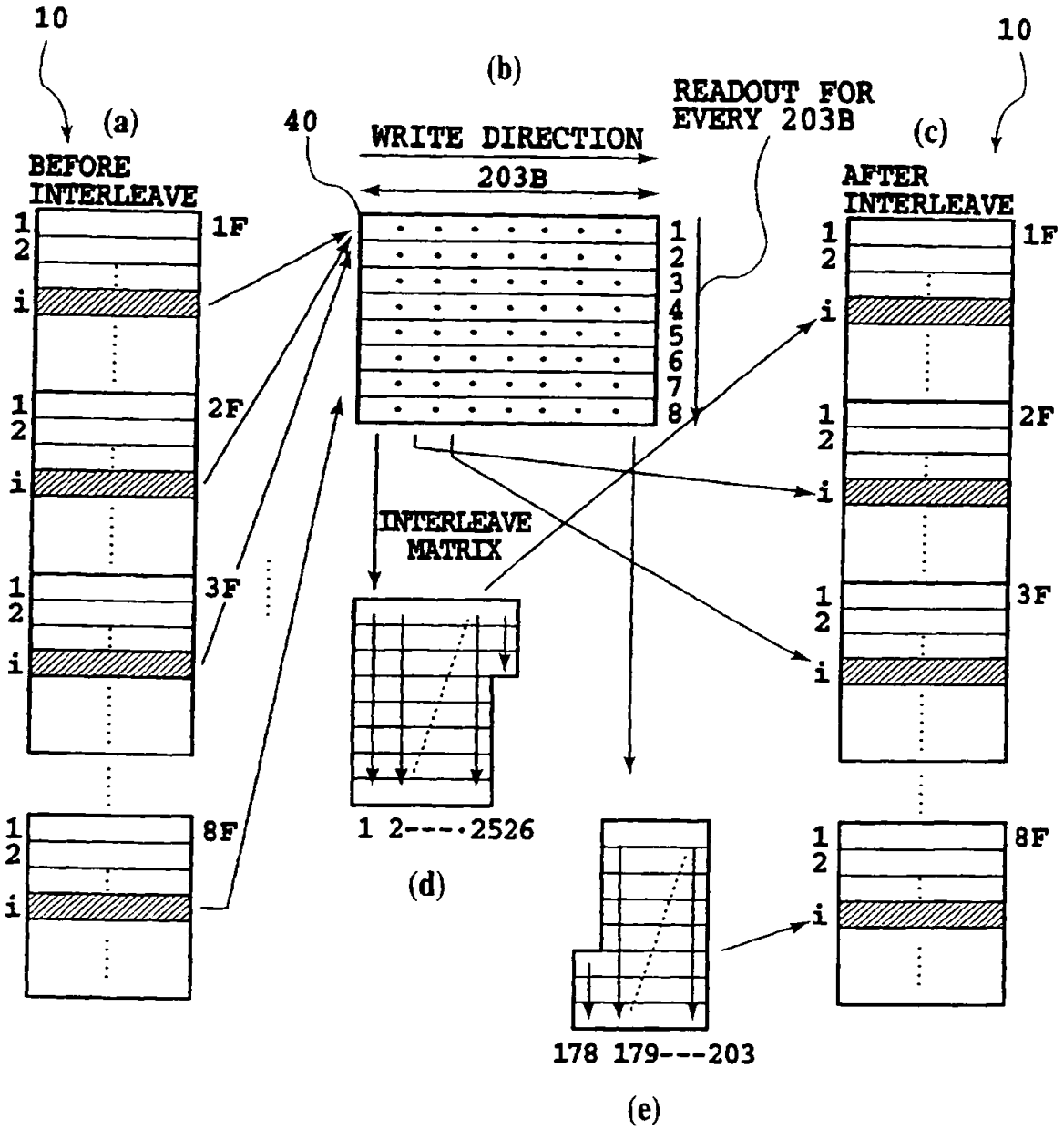

FIG.3

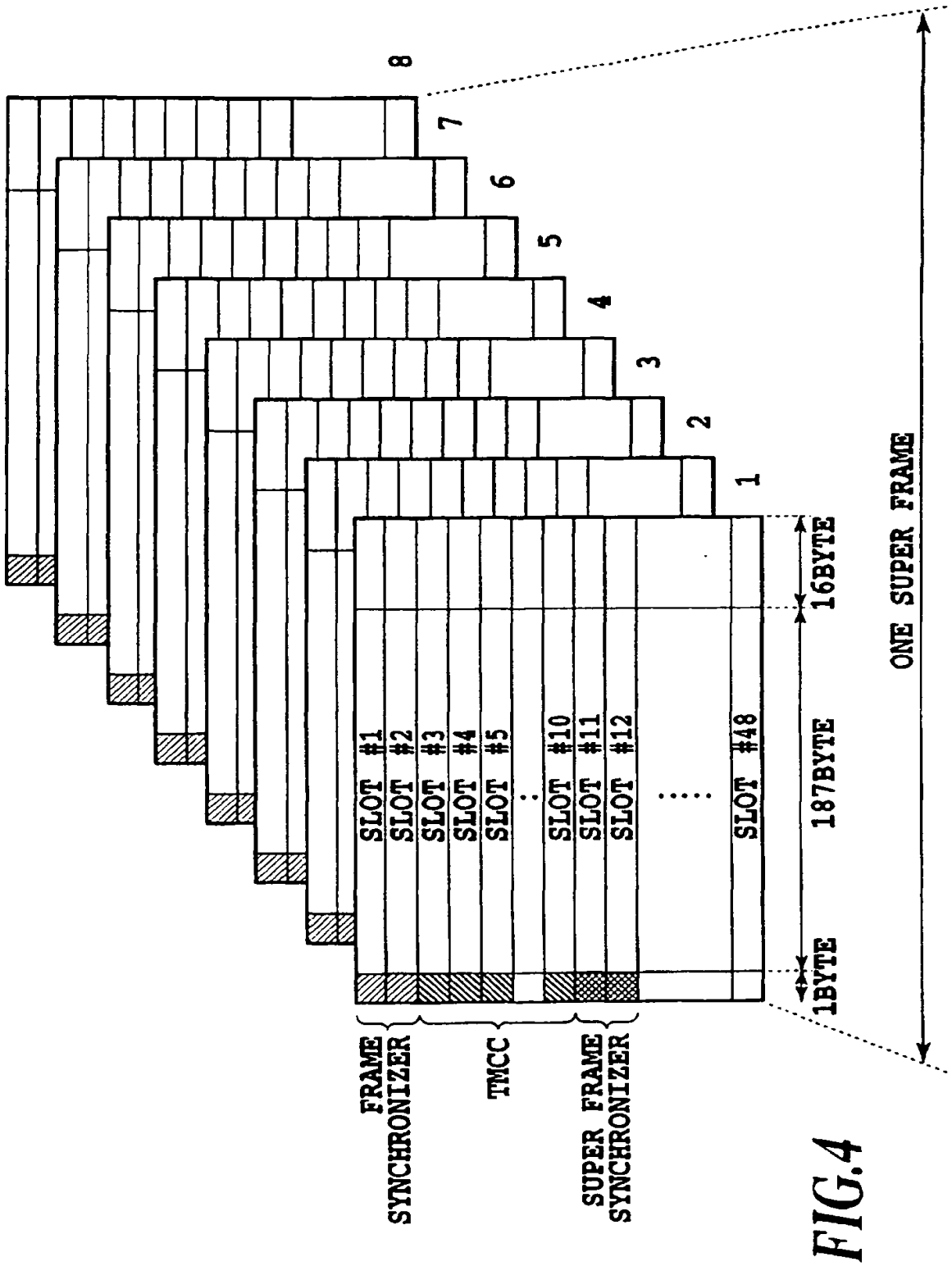

FIG.4

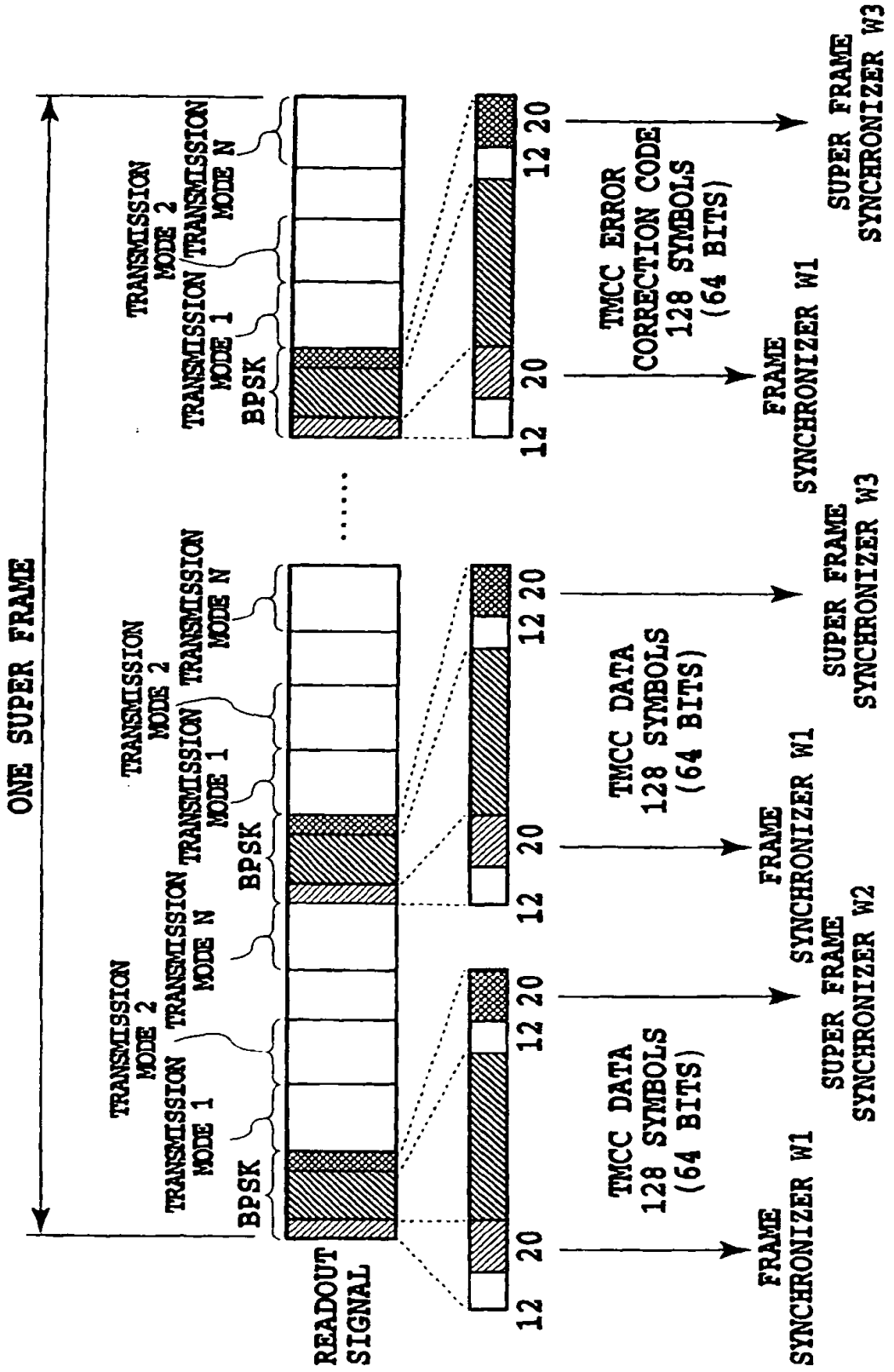

FIG.5

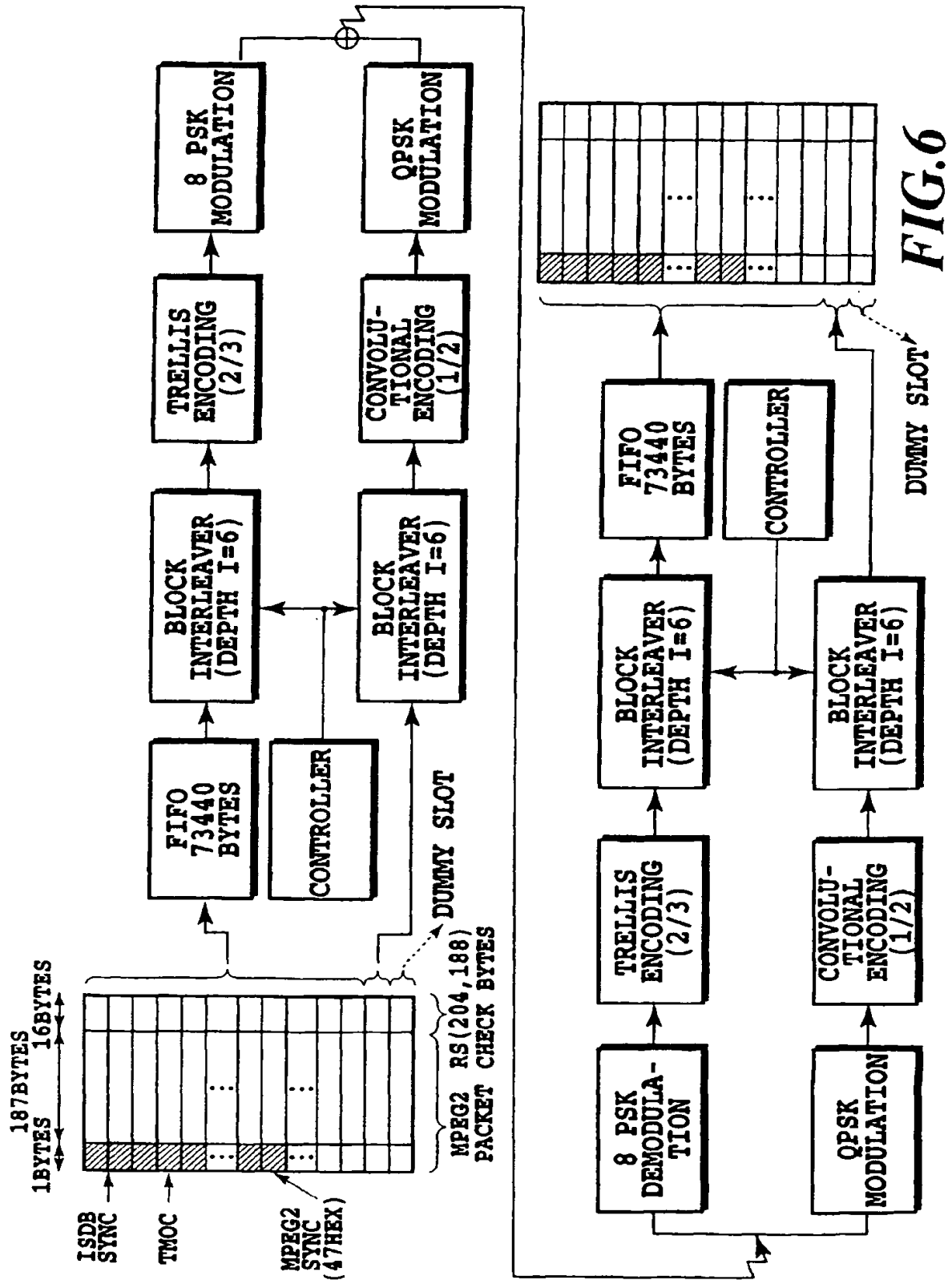

FIG.6

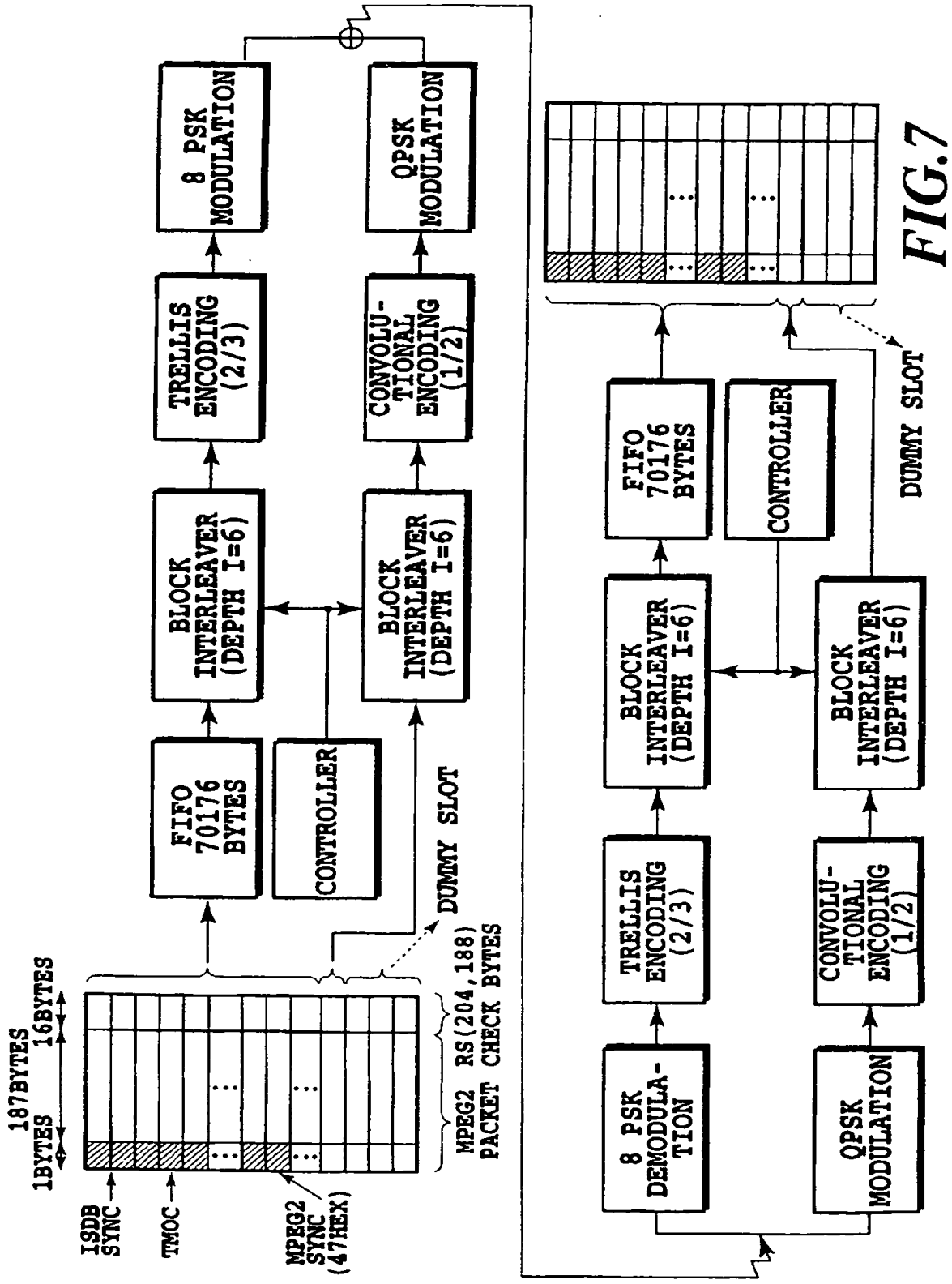

FIG.7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/05680

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[6] H04L1/00, H04J3/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[6] H04L1/00, H04J3/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1997
Kokai Jitsuyo Shinan Koho 1971-1999

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Hisakazu Katou (Hisakazu), Akinori Hashimoto (Akinori) "12GHz tai eisei ISDB heno kaisou densou no tekiyou", Technical Report of the Institut of Television Engineers of Japan, Vol. 20, No. 22, pages 11 to 16, BCS'94-14 (Mar. 1996), Page 15, right column, line 1 to last line ; Figs. 6, 7 ; Tables 6, 8, 9	1, 2
A	Hisakazu Katou (Hisakazu), Akinori Hashimoto (Akinori), et al., "Eisei ISDB densou houshiki no kentou", Eizou Jouhou Media Gakkai Gijutsu Houkoku, Vol. 21, No. 25, pages 1 to 5, BCS'97-12 (Mar. 1997), Page 4, left column, lines 2 to 23 ; page 4, right column, line 19 to page 5, left column, line 4 ; Figs. 5 to 8	1, 2

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 March, 1999 (02. 03. 99)	16 March, 1999 (16. 03. 99)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)